



# STP24DP05

## 24-bit constant current LED sink driver with output error detection

### Features

- Low voltage power supply down to 3 V
- 8 x 3 constant current output channels
- Adjustable output current through external resistors
- Short and open output error detection
- Serial data IN/Parallel data OUT
- Shift register data flow registers control
- Accepts 3.3 V and 5 V micro driver
- Output current: 5-80 mA
- 25 MHz clock frequency
- High thermal efficiency package

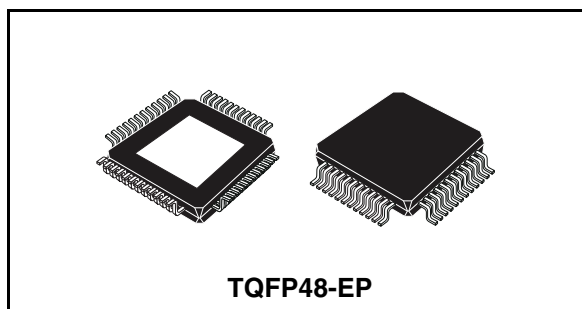
### Description

The STP24DP05 is a monolithic, low voltage, low current power 24-bit shift register designed for LED panel displays. The device contains a 8 x 3-bit serial-in, parallel-out shift register that feeds a 8 x 3-bit D-type storage register. In the output stage, twenty-four regulated current sources were designed to provide 5-80 mA constant current to drive the LEDs.

The 8 x 3 shift registers data flow sequence order can be managed with two dedicated pins.

The STP24DP05 has a dedicated pin to activate the outputs with a sequential delay, that will prevent inrush current during outputs turn-ON.

The device detection circuit checks 3 different conditions that can occur on the output line: short to GND, short to  $V_O$  or open line.



The data detection results are loaded in the shift registers and shifted out via the serial line output.

The detection functionality is activated with a dedicated pin or as alternative, through a logic sequence that allows the user to enter or exit from detection mode.

Through three external resistors, users can adjust the output current for each 8-channel group, controlling in this way the light intensity of LEDs.

The STP24DP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series.

The high clock frequency, 25 MHz, makes the device suitable for high data rate transmission.

The 3.3 V of voltage supply is useful for applications that interface any micro from 3.3 V.

**Table 1. Device summary**

Order code	Package	Packaging
STP24DP05BTR	TQFP48-EP <sup>(1)</sup>	Tape and reel

1. Thermal pad size: 3.5 mm x 3.5 mm

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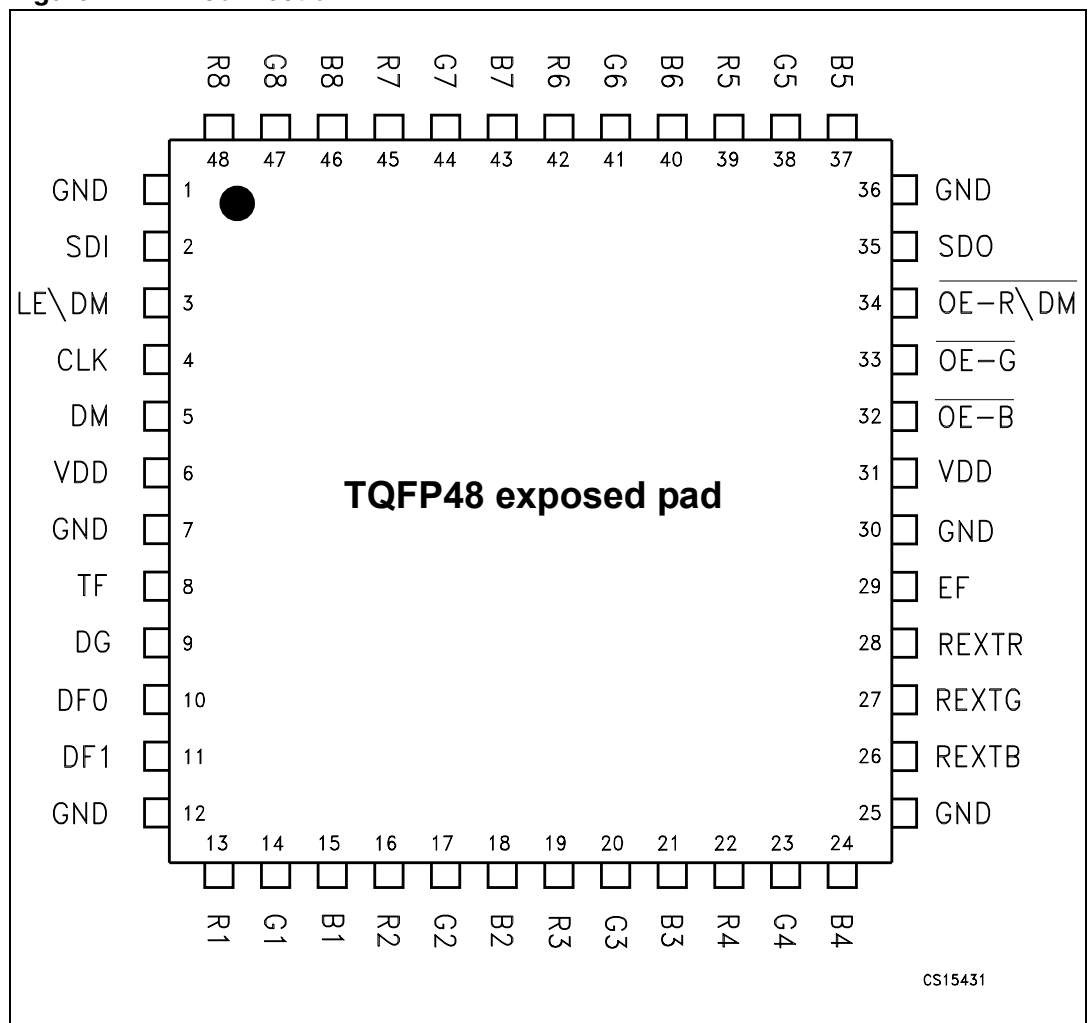
# 1 Summary description

**Table 2. Current accuracy**

Output voltage	Typical current accuracy		Output current	V <sub>DD</sub>	Temperature
	Between bits	Between ICs			
≥ 1.0 V	± 3 %	± 6 %	≥ 15 to 80 mA	3.3 V to 5 V	25 °C
≥ 0.2 V	± 6 %	± 6 %	5 to 15 mA		

## 1.1 Pin connection and description

**Figure 1. Pin connection**



*Note:* The exposed pad is electrically not connected

**Table 3. Pin description**

Pin N°	Symbol	Name and function
1, 7, 12, 25, 30, 36	GND	Ground terminal
2	SDI	Serial data input
35	SDO	Serial data output
4	CLK	Clock for serial data
3	LE\DM	Data latch in both SH register
5	DM	Detection mode pin
13, 16, 19, 22, 39, 42, 45, 48	R1 - 8	8 channel LED driver outputs
8	TF	Thermal flag (open drain)
29	EF	Error detection flag (open drain)
9	DG	Gradual delay
15, 18, 21, 24 37, 40, 43, 46	B1 - 8	8 channel LED driver outputs
32	$\overline{OE-B}$	Output enable for B1 - 8
33	$\overline{OE-G}$	Output enable for G1 - 8
34	$\overline{OE-R\backslash DM}$	Output enable for R1 - 8
28	REXTR	Control outputs R1 - 8
27	REXTG	Control outputs G1 - 8
26	REXTB	Control outputs B1 - 8
14, 17, 20, 23 38, 41, 44, 48	G1 - 8	8 channel LED driver outputs
10	DF0	Data banks flow bit 0
11	DF1	Data banks flow bit 1
31	VDD	Supply voltage terminal

## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage - digital	0 to 7	V
$V_O$	Output voltage - LED driver	-0.5 to 20	V
$V_{TF}$ and $V_{ER}$	Open drain absolute voltage	0 to 7	V
$I_O$	Output current - LED driver	80	mA
$V_I$	Input voltage - digital	-0.4 to $V_{DD}+0.4$	V
$I_{GND}$	GND terminal current	2000	mA
$f_{CLK}$	Clock frequency	30	MHz

### 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Value	Unit
$T_{OPR}$	Operating temperature range	-40 to 125	°C
$T_{STG}$	Storage temperature range	-40 to 150	°C
$R_{thJA}$	Thermal resistance junction-ambient <sup>(1)</sup> <sup>(2)</sup>	33	°C/W

1. The exposed pad should be soldered directly to the PCB to realize the thermal benefits.
2. Packages tested on multi-layer (1S2P) JEDEC compliant test boards

## 2.3 Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{DD}$	Supply voltage		3.0		5.5	V
$V_O$	Output voltage				20	V
$I_O$	Output current	OUTn	5		80	mA
$I_{OH}$	Output current	SERIAL-OUT		+10		mA
$I_{OL}$	Output current	SERIAL-OUT		-10		mA
$V_{IH}$	Input voltage		$0.7V_{DD}$		$V_{DD}+0.3$	V
$V_{IL}$	Input voltage		-0.3		$0.3V_{DD}$	V
$t_{wLAT}$	LE pulse width	$V_{DD} = 3.0\text{ V to }5.0\text{ V}$	15			ns
$t_{wCLK}$	CLK pulse width		15			ns
$t_{wEN}$	$\overline{OE}$ pulse width		150			ns
$t_{SETUP(D)}$	Setup time for DATA		15			ns
$t_{HOLD(D)}$	Hold time for DATA		5			ns
$t_{SETUP(L)}$	Setup time for LATCH		10			ns
$f_{CLK}$	Clock frequency		Cascade operation <sup>(1)</sup>			25

1. If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

### 3 Electrical characteristics

**Table 7. Electrical characteristics**  
( $V_{DD} = 3.3\text{ V to }5\text{ V}$ ,  $T = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IH}$	Input voltage high level		$0.7V_{DD}$		$V_{DD}$	V
$V_{IL}$	Input voltage low level		GND		$0.3V_{DD}$	V
$I_{OH}$	Output leakage current	$V_{OH} = 20\text{ V}$			10	$\mu\text{A}$
$V_{OL}$	Output voltage (Serial-OUT)	$I_{OL} = 1\text{ mA}$			0.4	V
$V_{OH}$	Output voltage (Serial-OUT)	$I_{OH} = -1\text{ mA}$	$V_{DD}-0.4\text{V}$			V
$I_{OL1}$	Output current	$V_O = 0.3\text{ V}$ , $R_{EXT} = 2\text{ k}\Omega$ , $I_O = 10\text{ mA}$		20		mA
$I_{OL2}$		$V_O = 0.3\text{ V}$ , $R_{EXT} = 1\text{ k}\Omega$ , $I_O = 20\text{ mA}$		80		mA
$I_{OL3}$		$V_O = 0.3\text{ V}$ , $R_{EXT} = 250\ \Omega$ , $I_O = 80\text{ mA}$		80		mA
$\Delta I_{OL1}$	Output current error among the channels (All outputs ON)	$V_O = 0.3\text{ V}$ , $R_{EXT} = 2\text{ k}\Omega$ , $I_O = 10\text{ mA}$		$\pm 2$	$\pm 3$	%
$\Delta I_{OL2}$		$V_O = 0.3\text{ V}$ , $R_{EXT} = 1\text{ k}\Omega$ , $I_O = 20\text{ mA}$		$\pm 2$	$\pm 3$	%
$\Delta I_{OL3}$		$V_O = 0.3\text{ V}$ , $R_{EXT} = 250\ \Omega$ , $I_O = 80\text{ mA}$		$\pm 2$	$\pm 3$	%
$R_{SIN(up)}$	Pull-up resistor		300	600	800	$\text{k}\Omega$
$R_{SIN(down)}$	Pull-down resistor		300	400	500	$\text{k}\Omega$
$LE_{(up)}$ $DG_{(up)}$ $OE-R\backslash$ $DM_{(up)}$ $OE-G_{(up)}$ $OE-B_{(up)}$ $DF0$ $DF1$	Pull-up resistor		300	400	500	$\text{k}\Omega$
$I_{DD(OFF1)}$	Supply current (OFF)	$R_{EXT} = 1\text{ k}\Omega$ OUT 0 to 15 = OFF		9	12	mA
$I_{DD(OFF2)}$		$R_{EXT} = 250\ \Omega$ OUT 0 to 15 = OFF		32	40	
$I_{DD(ON1)}$	Supply current (ON)	$R_{EXT} = 1\text{ k}\Omega$ OUT 0 to 15 = ON		13	18	
$I_{DD(ON2)}$		$R_{EXT} = 250\ \Omega$ OUT 0 to 15 = ON		35	40	

**Table 7. Electrical characteristics (continued)**  
( $V_{DD} = 3.3\text{ V to }5\text{ V}$ ,  $T = 25\text{ }^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Thermal	Thermal protection			170		$^\circ\text{C}$
$V_{TF}$	Output voltage				5	V
$I_{TF}$	Output current	$V_{TF} @ 1\text{ V}$	20			mA
$V_{EF}$	Output voltage				5	V
$I_{EF}$	Output current	$V_{EF} @ 1\text{ V}$	20			mA

**Table 8. Switching characteristics ( $V_{DD} = 5\text{ V}$ ,  $T = 25\text{ }^\circ\text{C}$ , unless otherwise specified.)**

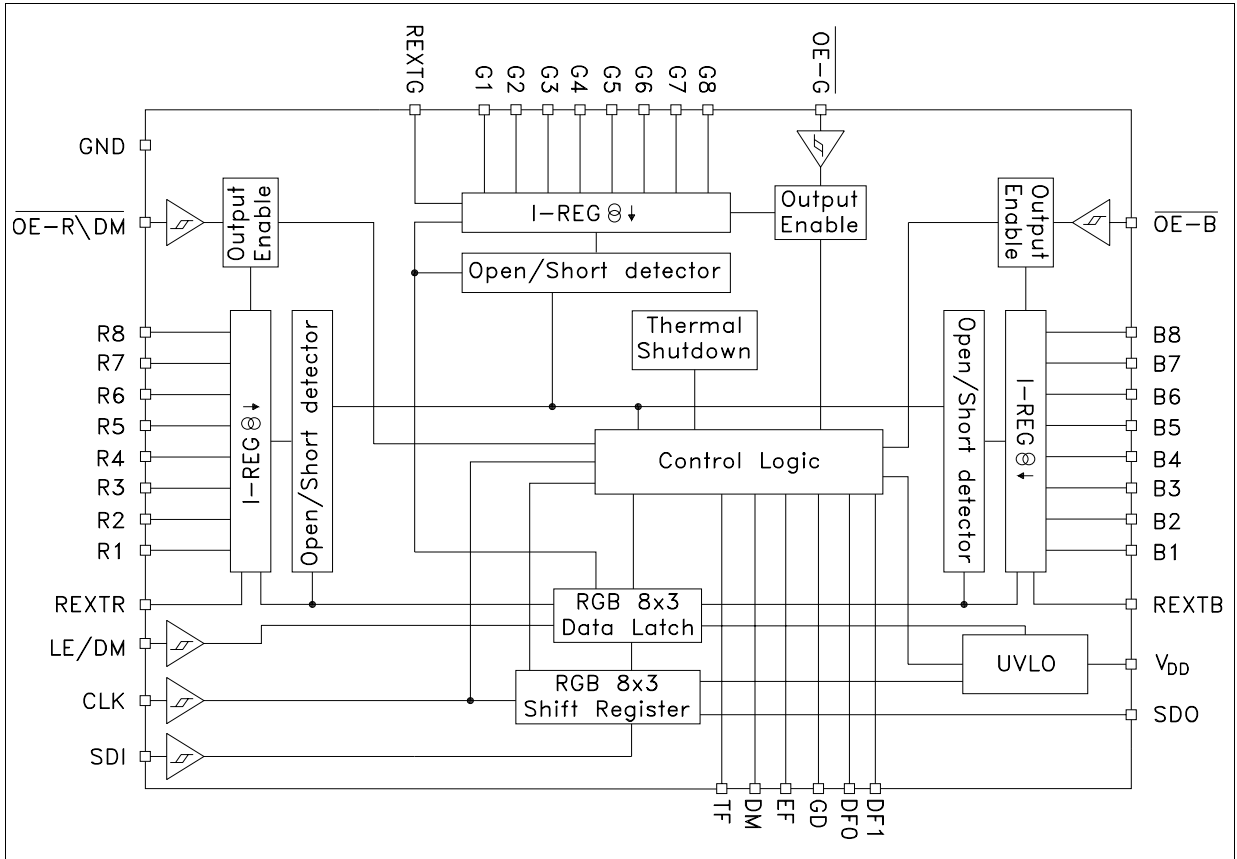
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{PLH1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE = H, $\overline{\text{OE}} = \text{L}$	$V_{DD} = 3.3\text{ V}$		62	100	ns
		$V_{DD} = 5\text{ V}$		38	60	
$t_{PLH2}$	Propagation delay time, LE- $\overline{\text{OUTn}}$ , $\overline{\text{OE}} = \text{L}$	$V_{DD} = 3.3\text{ V}$		67	107	ns
		$V_{DD} = 5\text{ V}$		44	60	
$t_{PLH3}$	Propagation delay time, $\overline{\text{OE}}-\overline{\text{OUTn}}$ , LE = H	$V_{DD} = 3.3\text{ V}$		65	83	ns
		$V_{DD} = 5\text{ V}$		38	45	
$t_{PLH}$	Propagation delay time, CLK-SDO	$V_{DD} = 3.3\text{ V}$	14	22	36	ns
		$V_{DD} = 5\text{ V}$	9	14	23	
$t_{PHL1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE = H, $\overline{\text{OE}} = \text{L}$	$V_{DD} = 3.3\text{ V}$		46	70	ns
		$V_{DD} = 5\text{ V}$		39	50	
$t_{PHL2}$	Propagation delay time, LE- $\overline{\text{OUTn}}$ , $\overline{\text{OE}} = \text{L}$	$V_{DD} = 3.3\text{ V}$		51	76	ns
		$V_{DD} = 5\text{ V}$		46	55	
$t_{PHL3}$	Propagation delay time, $\overline{\text{OE}}-\overline{\text{OUTn}}$ , LE = H	$V_{DD} = 3.3\text{ V}$		41	45	ns
		$V_{DD} = 5\text{ V}$		33	39	
$t_{PHL}$	Propagation delay time, CLK-SDO	$V_{DD} = 3.3\text{ V}$	15	24	38	ns
		$V_{DD} = 5\text{ V}$	9	15	24	
$t_{ON}$	Output rise time 10~90% of voltage waveform	$V_{DD} = 3.3\text{ V}$		33	57	ns
		$V_{DD} = 5\text{ V}$		17	27	
$t_{OFF}$	Output fall time 90~10% of voltage waveform	$V_{DD} = 3.3\text{ V}$		24	34	ns
		$V_{DD} = 5\text{ V}$		25	37	
$t_r$	CLK rise time <sup>(1)</sup>				5000	ns
$t_f$	CLK fall time <sup>(1)</sup>				5000	ns

1. In order to achieve high cascade data transfer, please consider  $t_r/t_f$  timings carefully.



# 4 Block diagram

Figure 2. Block diagram



## 5 Equivalent circuit and outputs

Figure 3.  $\overline{OE}xx$  terminal

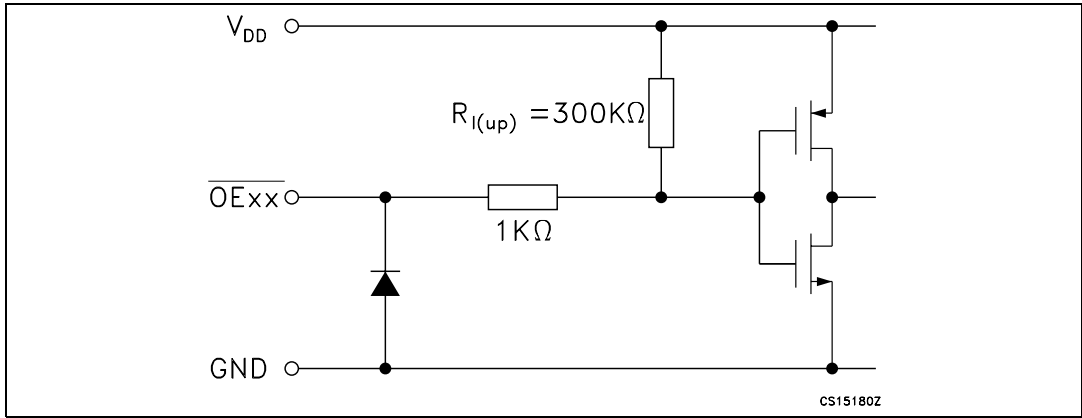


Figure 4.  $LE\backslash DM$  terminal

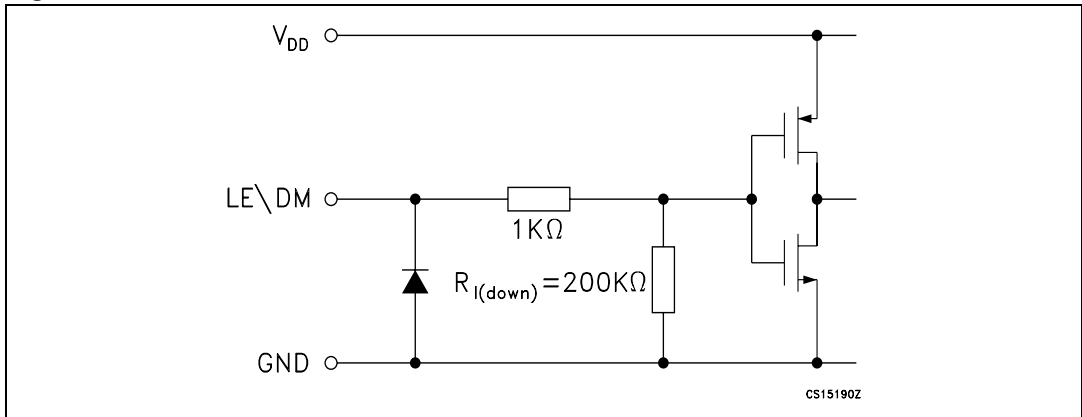


Figure 5. CLK, SDI terminal

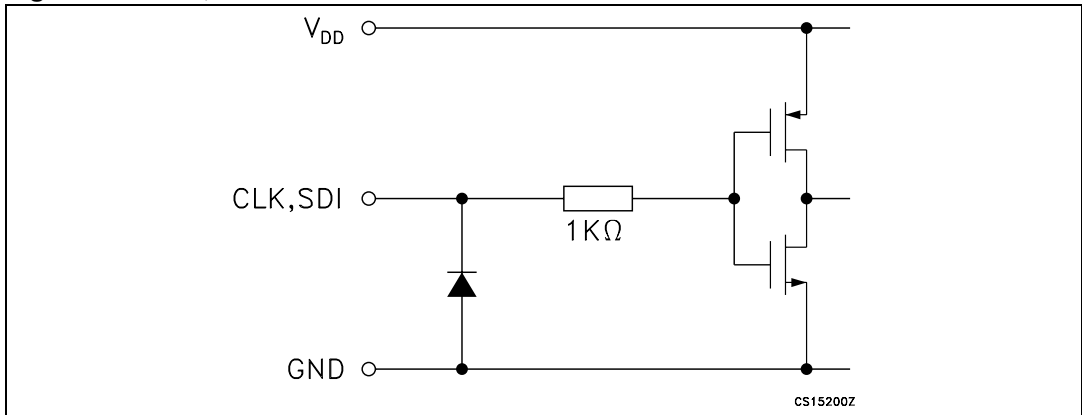


Figure 6. SDO terminal

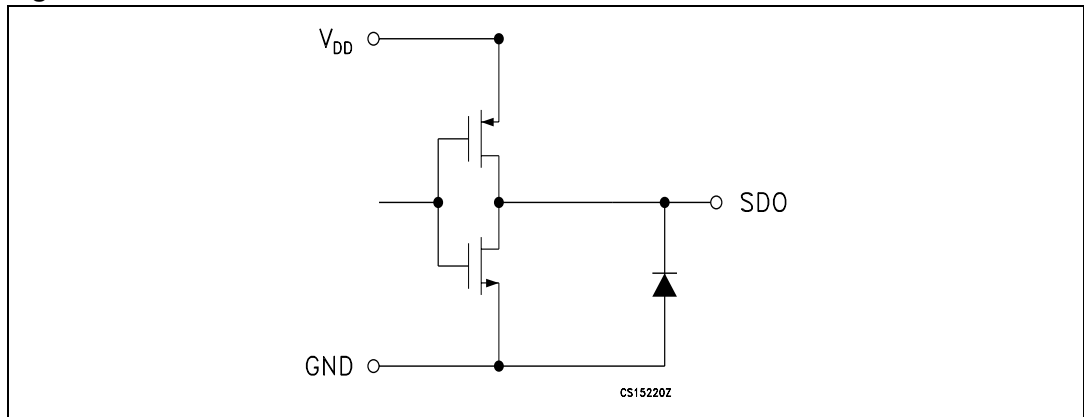
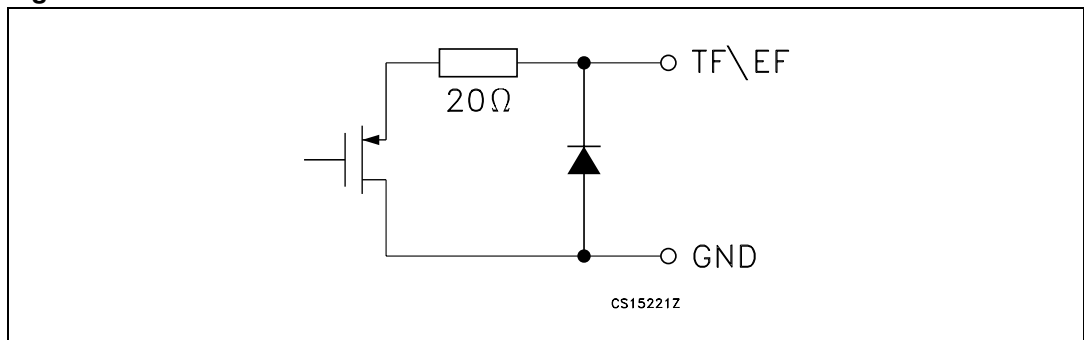
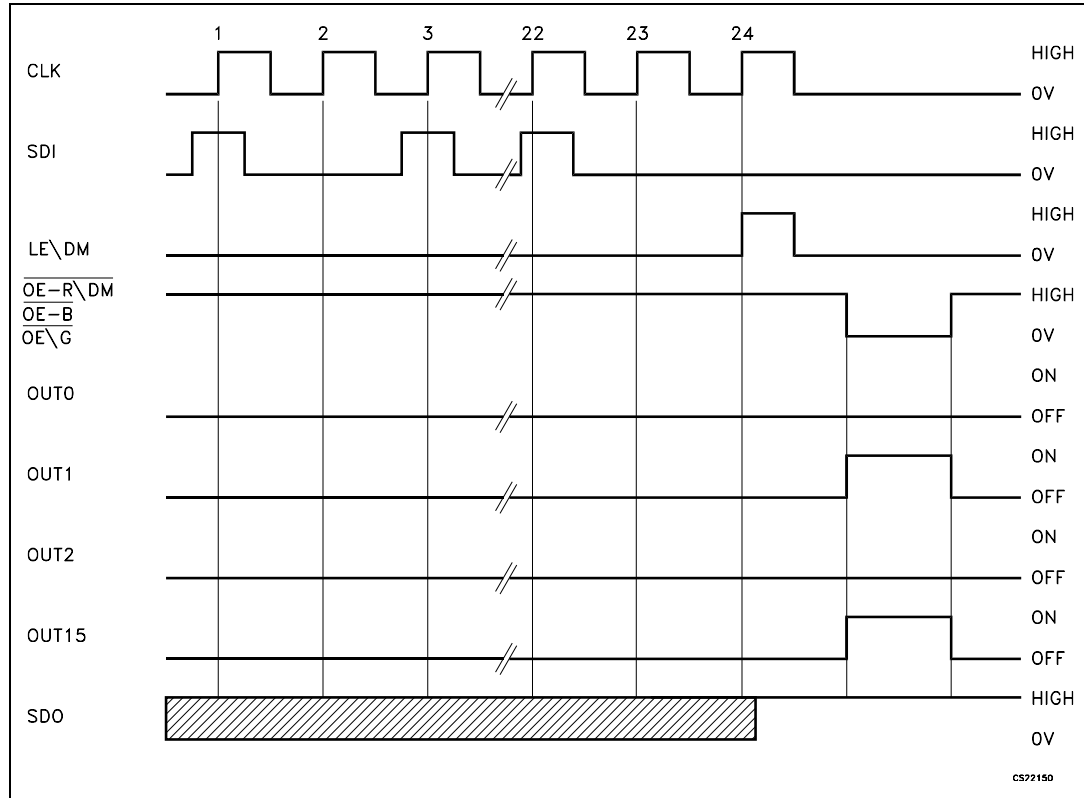


Figure 7. TF and EF



## 6 Timing diagrams

Figure 8. Timing diagram



Note: The latches circuit holds data when the LE terminal is low.

- 1 When LE\DM terminal is at high level, latch circuit hold the data it passes from the input to the output.
- 2 When either  $\overline{OE-R\ DM}$ ,  $\overline{OE-G}$ ,  $\overline{OE-B}$  terminals are at low level, output terminals R\G\B1 to R\G\B8 respond to the data, either ON or OFF.
- 3 When either  $\overline{OE-R\ DM}$ ,  $\overline{OE-G}$ ,  $\overline{OE-B}$  terminals are at high level, it switches off all the data on the output terminal R\G\B1 to R\G\B8.

Figure 9. Clock, serial-in, serial-out

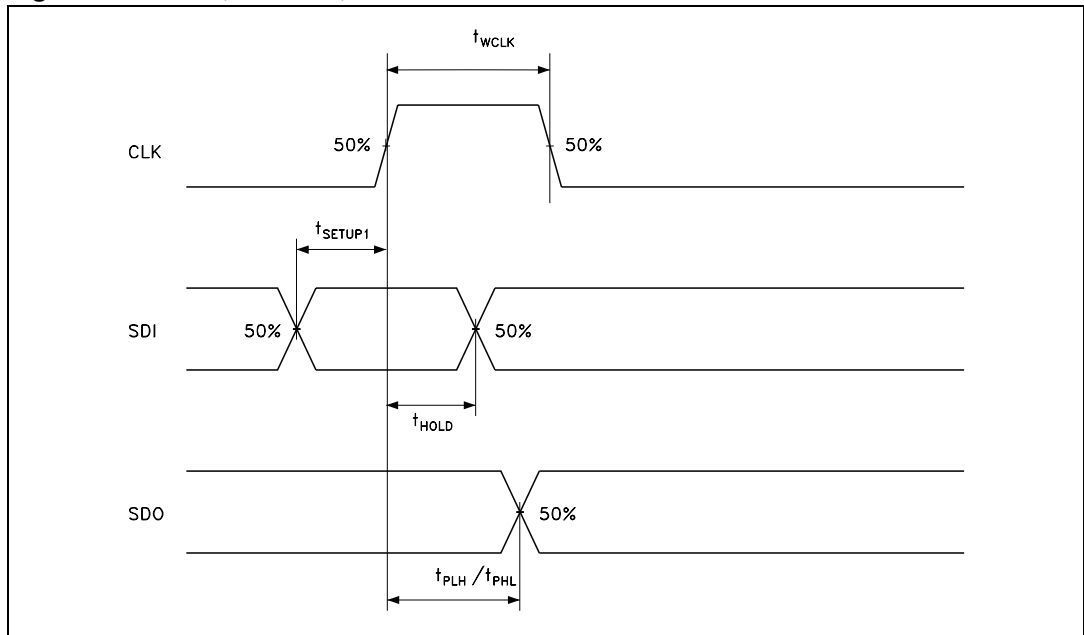


Figure 10. Clock, serial-in, latch, enable, outputs

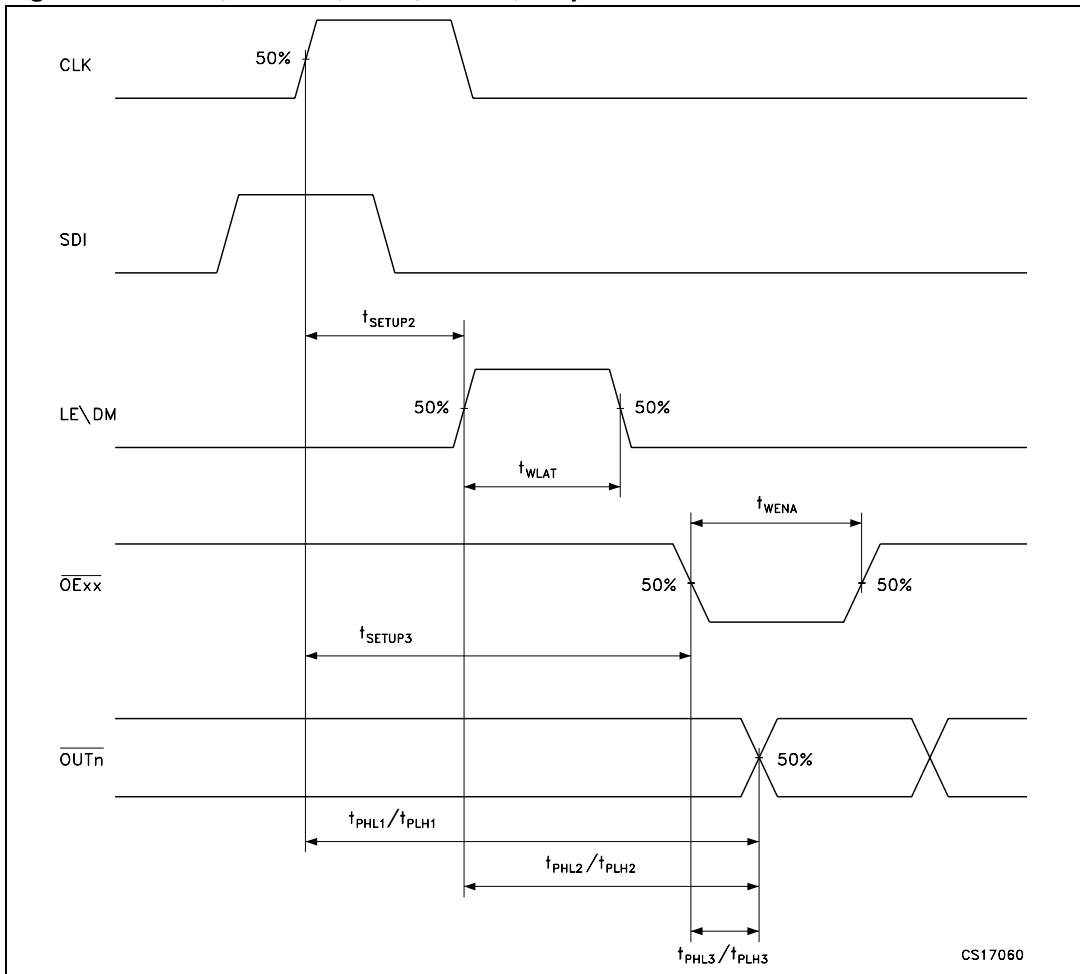
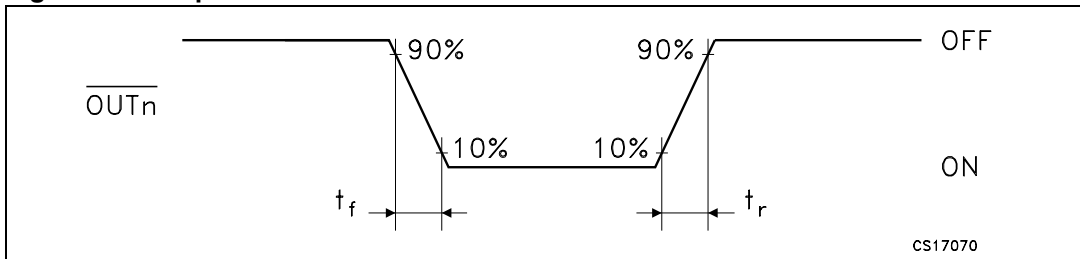


Figure 11. Outputs



## 7 Feature description

### 7.1 DG: gradual outputs delay

This feature prevents large inrush current and reduces the bypass capacitors.

The fixed delay time can be activated with DG = LOW and the typical output delay is 20 ns for each group of 8 outputs R, G, B. Eg: R1, G1, B1 has no delay, R2, G2, B2 has 20 ns delay and R3, G3, B3, has 40 ns delay, etc.

**Table 9. Typical gradual delay time table**

Delay time (ns) from $\overline{\text{OE}}_{\text{xx}}$	R1 G1 B1	R2 G2 B2	R3 G3 B3	R4 G4 B4	R5 G5 B5	R6 G6 B6	R7 G7 B7	R8 G8 B8
DG = 0	0	30	60	90	120	150	180	200
DG = 1		0	0	0	0	0	0	0

### 7.2 Error detection condition

**Table 10. Detection conditions ( $V_{\text{DD}} = 3.3$  to  $5$  V,  $I_{\text{O}} = 20$  mA,  $t_{\text{A}} = 25$  °C)**

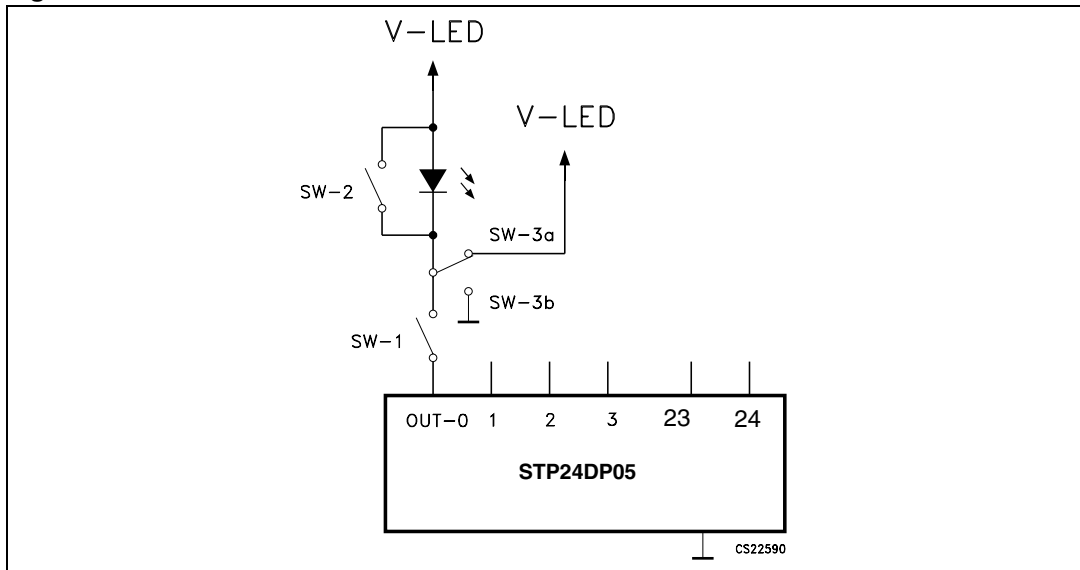
<b>SW-1 Open or SW-3b</b>	Open line or output short to GND detected	$\Rightarrow I_{\text{ODEC}} \leq 0.4 \times I_{\text{O}}$	No error detected	$\Rightarrow I_{\text{ODEC}} \geq 0.35 \times I_{\text{O}}$
<b>SW-2 Closed or SW-3a</b>	Short on LED or short to V-LED detected	$\Rightarrow V_{\text{O}} \geq 2.6$ V	No error detected	$\Rightarrow V_{\text{O}} \leq 2.4$ V

Note:  $I_{\text{O}}$  = the output current programmed by the  $R_{\text{EXT}}$   
 $I_{\text{ODEC}}$  = the detected output current in detection mode

**Table 11. Typical current threshold values to detect LED open line**

Iset (mA)	Rext ( $\Omega$ )	Typ. out current detection (mA)
5	3920	1.28
10	1960	2.45
20	980	7.4
50	386	17
80	241	27

Figure 12. Detection circuit



### 7.3 Phase one: “entering in detection mode”

From the “normal mode” condition the device can switch to the “error detection mode” by a DM PIN set to LOW or a logic sequence on the OE-R/DM and LE/DM pins as showed in the following table and diagram:

Figure 13. EDM timing diagram using DM pin

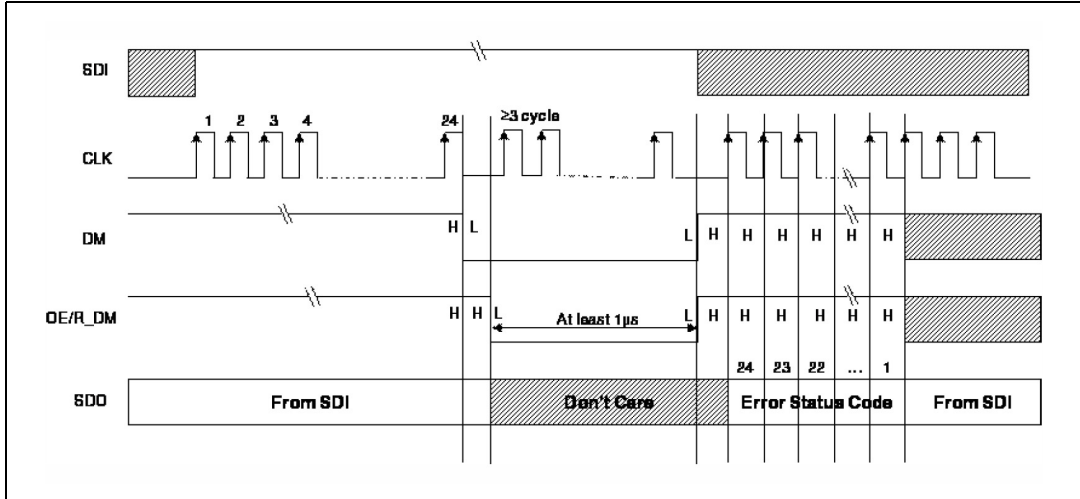
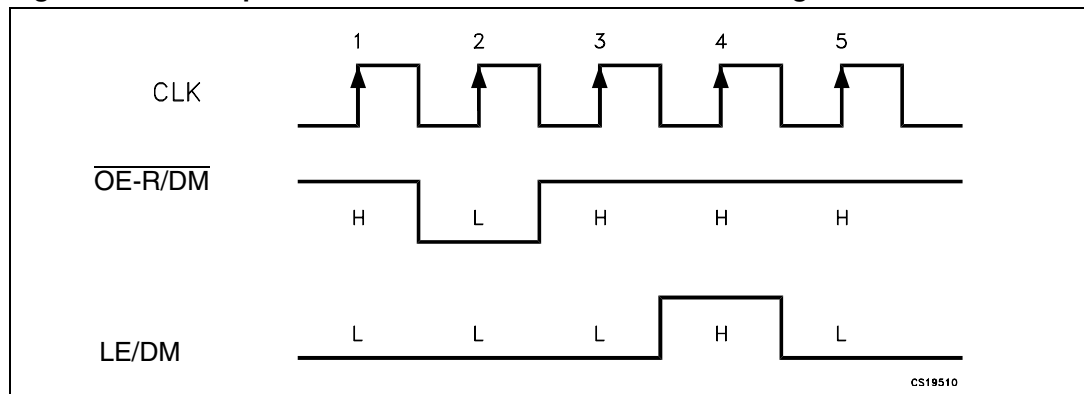


Table 12. SPI sequence to enter in detection mode - truth table

CLK	1°	2°	3°	4°	5°
$\overline{\text{OE-R/DM}}$	H	L	H	H	H
LE/DM	L	L	L	H	L



Figure 14. SPI sequence to enter in detection mode - time diagram

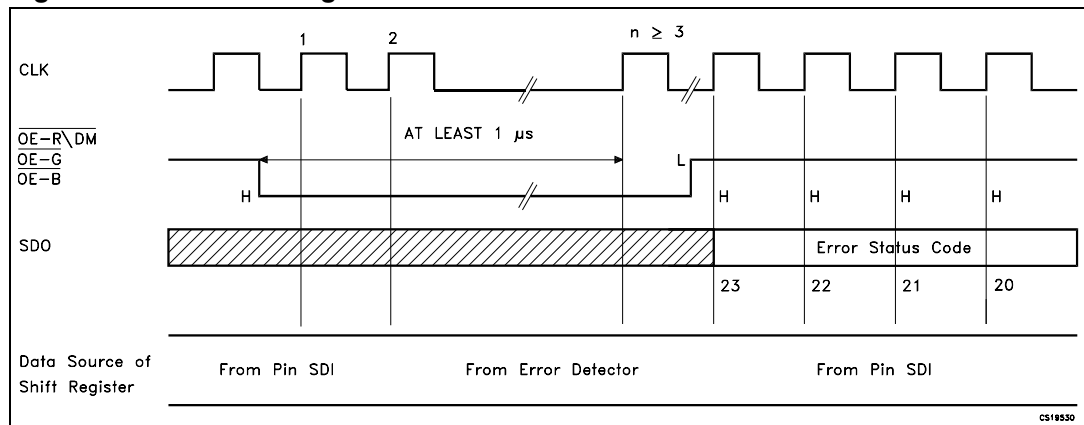


After these five CLK cycles the device goes into the “error detection mode” and at the 6<sup>th</sup> rise front of CLK the SDI data are ready for the sampling.

### 7.4 Phase two: “error detection”

The eight data bits must be set “1” in order to set ON all the outputs during the detection. The data are latched by LE/DM and after that the outputs are ready for the detection process. When the micro controller switches the OE-R/DM to LOW, the device drives the LEDs in order to analyze if an OPEN or SHORT condition has occurred.

Figure 15. Detection diagram



The LEDs status will be detected at least in 1 microsecond and after this time the microcontroller sets OE-R/DM in HIGH state and the output data detection result will go to the microprocessor via SDO.

Detection mode and normal mode use both the same format data. As soon as all the detection data bits are available on the serial line, the device may go back to normal mode of operation.

## 7.5 Phase three: “resuming to normal mode”

In order to re-enter in normal mode either the LE\DM pin or the sequence showed in the following table and diagram can be used:

**Table 13. SPI sequence to resume in normal mode - truth table**

CLK	1°	2°	3°	4°	5°
$\overline{\text{OE-R/DM}}$	H	L	H	H	H
LE/DM	L	L	L	L	L

*Note:* For proper device operation the “entering in detection” sequence must be followed by a “resume mode” sequence, it is not possible to insert consecutive equal sequence.

## 7.6 Shift registers data flow control

The 8x3 shift registers have a default RGB sequence serial data flow as showed on block diagram [Figure 2](#).

The data can be redirected by DF0 and DF1 pins, these pins change the order of the data flow according to the following table:

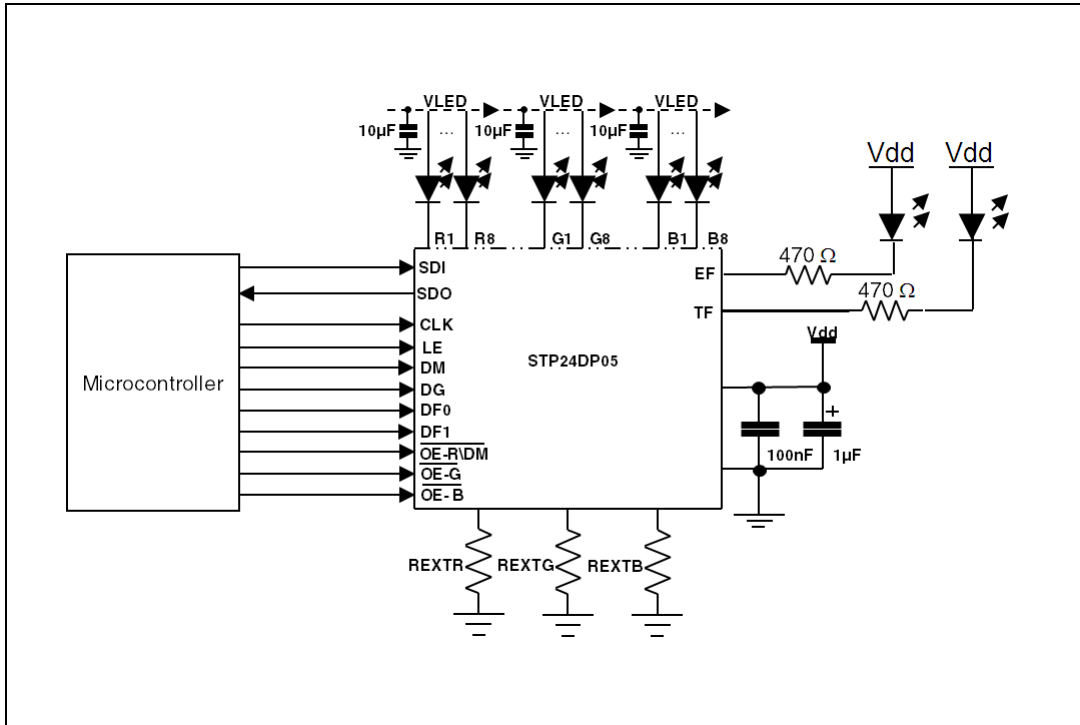
**Table 14. Shifter register data flow control**

Sequence	DF0	DF1
BGR	1	1
BGR	0	1
RGB	1	0
GBR	0	0

## 7.7 EFLAG/TFLAG - output detection and overtemperature monitoring

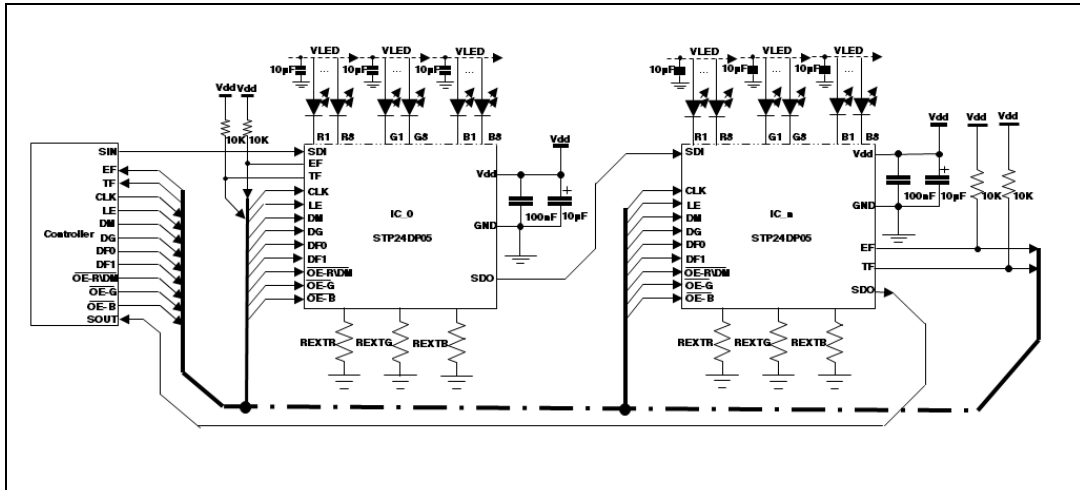
The open-drain output EFLAG and TFLAG are used to report the STP24DP05 error flags. During normal operating conditions, the voltage on EFLAG/TFLAG is pulled-up through an external resistor. When an error is detected, the internal switch is turned on, to GND.

Figure 16. TF and EF test circuit



# 8 Typical application schematic

Figure 17. Typical application schematic



## 9 Typical characteristics

Figure 18. Typical external resistor values vs output current capabilities

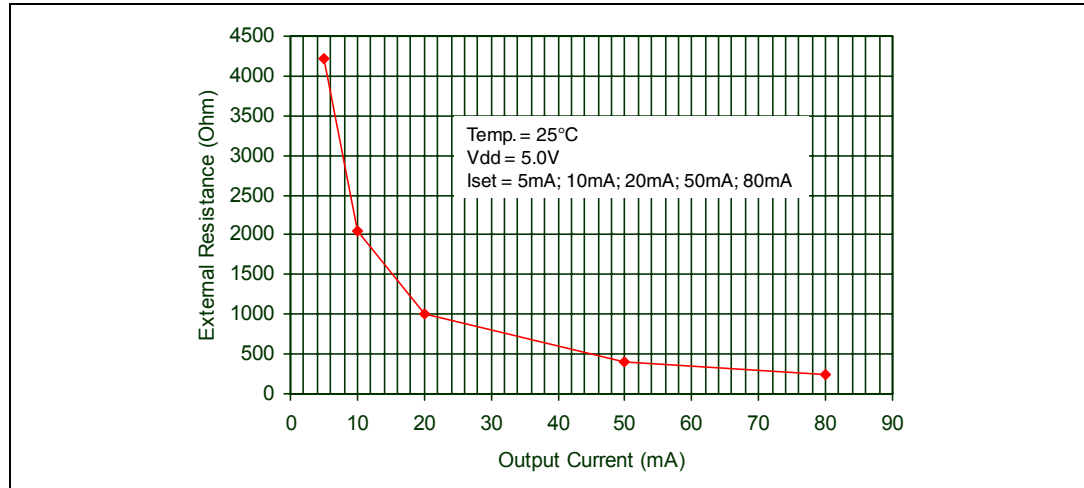


Table 15. Typical external resistor values vs output current capabilities

Iset	5 mA	10 mA	20 mA	50 mA	80 mA
Rext (Ω)	4210	2050	1000	400	249

Figure 19. Typical dropout voltage vs output current

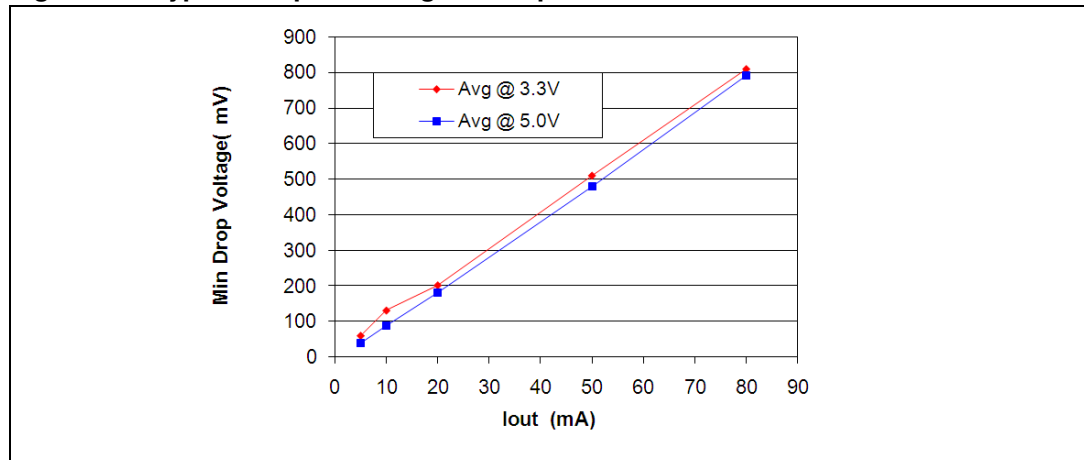


Table 16. Typical dropout voltage vs output current

Iset	Rext (Ω)	Avg (mV) @ 3.3 V	Avg (mV) @ 5.0 V
5	4210	59	41
10	2050	130	90
20	1000	201	180
50	400	500	480
80	249	810	790

## 10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Table 17. TQFP48-EP mechanical data**

Dim.	Min.	Typ.	Max
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
D2		3.50	
D3		5.50	
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
E2		3.50	
E3		5.50	
e		0.50	
L	0.45	0.60	0.75
L1		1.00	
k	0	3.5	7
ccc			0.08

Figure 20. TQFP48-EP mechanical data

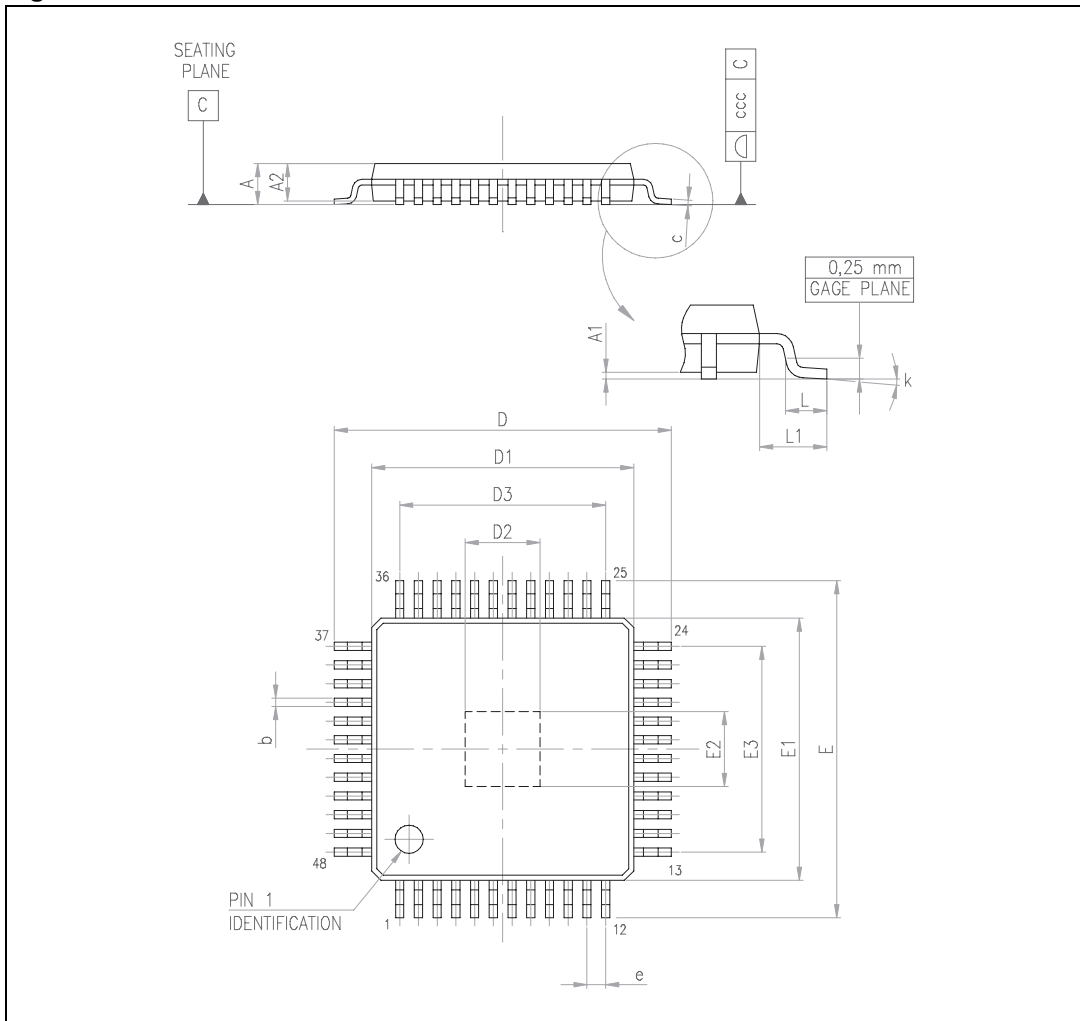
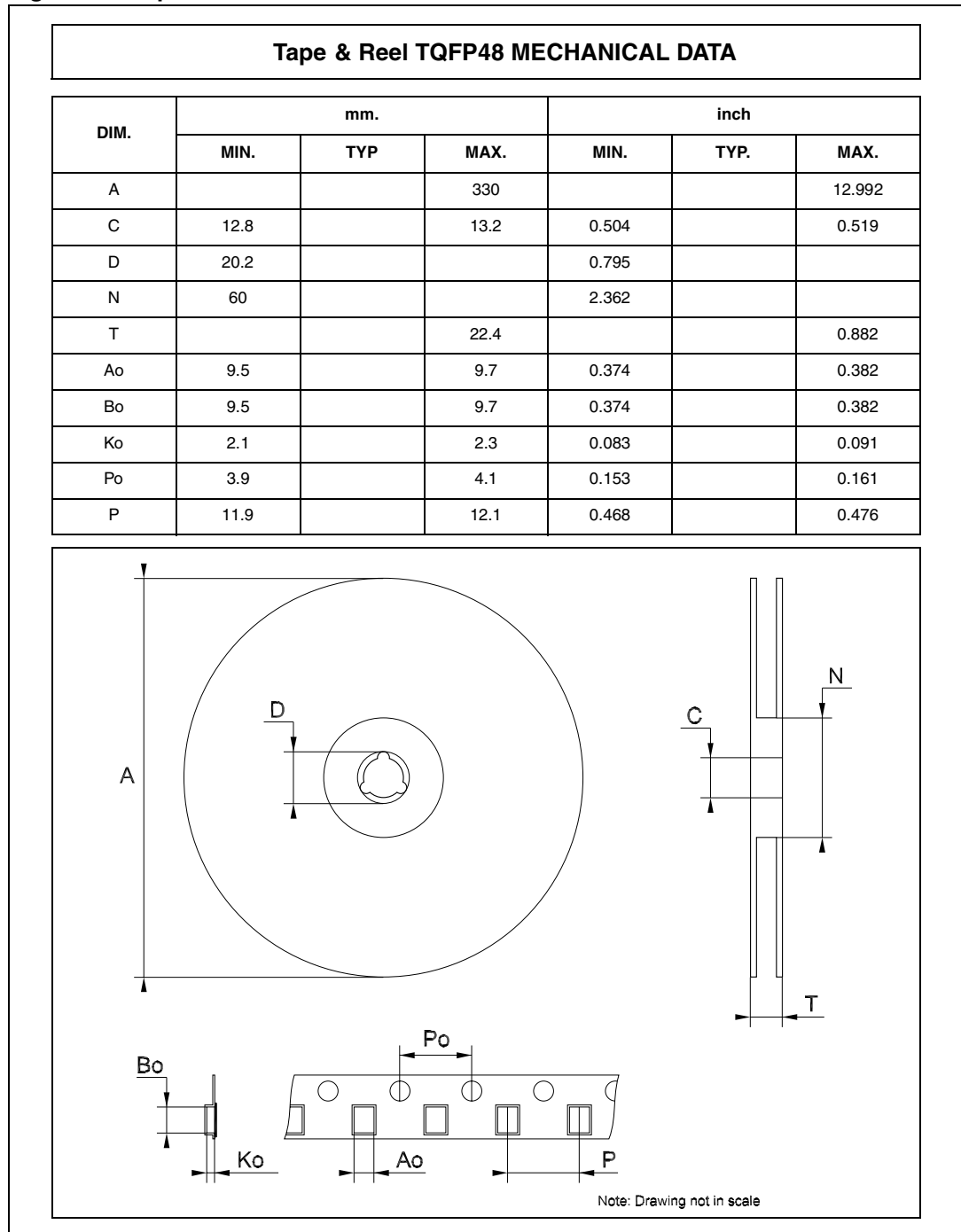


Figure 21. tape and reel TQFP48-EP





## 11 Revision history

**Table 18. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
19-Apr-2008	1	First release
12-Jan-2009	2	Updated package to TQFP48-EP
04-Mar-2009	3	Updated <a href="#">Table 3 on page 4</a>

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